IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	
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First Named Inventor: Gilbert Christopher Sih	:	**Confirmation No.** 3901
	:	
U.S. Patent Application No. 10/807,648	:	**Group Art Unit:** 2188
	:	
Filed: March 24, 2004	:	**Examiner:** Song, Jasmine

For: CACHED MEMORY SYSTEM AND CACHE CONTROLLER FOR EMBEDDED DIGITAL SIGNAL PROCESSOR

BRIEF ON APPEAL UNDER 37 C.F.R. § 41.37

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Further to the Notice of Appeal filed August 4, 2008, in connection with the above-identified application on appeal, the Appellant respectfully submits this Brief on Appeal. Please charge any fees or credit any overpayments that may be due with this Brief to Deposit Account No. 17-0026.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is QUALCOMM Incorporated, 5775 Morehouse Drive, San Diego, California, 92121.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals and/or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are a total of 35 claims pending in the instant application, namely claims 1-5, 7-8, 10-18 and 35-54. Claims 1, 12 and 14 are independent claims.

B. Status of All the Claims

1. Claims cancelled: 6, 9 and 19-34
2. Claims withdrawn from consideration but not cancelled: none
3. Claims pending: 1-5, 7-8, 10-18 and 35-54
4. Claims allowed: none
5. Claims rejected: 1-5, 7-8, 10-18 and 35-54

C. Claims on Appeal

Claims on appeal are claims 1-5, 7-8, 10-18 and 35-54 as rejected by the Final Office Action of 5/02/2008.

IV. STATUS OF AMENDMENTS

The Amendment filed January 25, 2008 (amending each of claims 1, 12, 14 and 47-48), has been entered, as indicated by the 5/02/2008 Final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is directed to an integrated circuit (IC) (e.g., see 300, 400, 920 of Figures 3, 4 and 9, respectively) including a processor core (e.g., see 330, 430 of Figures 3 and 4, respectively) operable to perform data processing for the integrated circuit, a cache memory (e.g., see 340, 440a/b/x of Figures 3 and 4, respectively) operable to store data for the processor core and an on-chip memory (e.g., see 350, 450 of Figures 3 and 4, respectively) operable to store data for the cache memory, wherein the cache memory is filled with data from the on-chip memory for cache misses, and wherein the on-chip memory is selectably filled with data from an external memory (e.g., see 360, 460 of Figures 3 and 4, respectively) independent of cache accesses of the cache memory under user control.

Claim 12 is directed to a wireless apparatus (900) including the integrated circuit of claim 1 and the external memory (e.g., see 360, 460 of Figures 3 and 4, respectively).

Claim 14 is directed to an integrated circuit (920), including a first processor (922) operable to perform general-purpose processing for the integrated circuit, a second processor (924) operable to perform data processing for the integrated circuit and including a processor core (e.g., see 330, 430 of Figures 3 and 4, respectively)operable to perform the data processing, and a first cache memory (e.g., see 340, 440a/b/x of Figures 3 and 4, respectively) operable to store data for the processor core, an on-chip memory (e.g., see 350, 450 of Figures 3 and 4, respectively) operable to store data for the first cache memory, wherein the first cache

memory is filled with data from the on-chip memory for cache misses, and wherein the on-chip memory is selectably filled with data from an external memory (e.g., see 360, 460 of Figures 3 and 4, respectively) independent of cache accesses of the first cache memory under user control and a first memory bus (e.g., see 928 of Figure 9) coupling the first and second processors to the external memory.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Examiner has finally rejected [i] claims 1, 12 and 14 under 35 U.S.C. 112, 1st paragraph for allegedly failing to comply with the Written Description requirement, [ii] claims 1-5, 7, 10-13, 35, 38-40, 43-46, 49 and 52-54 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,895,475 ("Volpe") in view of U.S. Patent No. 7,194,576 ("Boyle"), [iii] claim 8 under 35 U.S.C. 103(a) as being unpatentable over Volpe in view of Boyle and in further view of U.S. Publication No. 2004/0093479 ("Ramchandran"), [iv] claims 41-42 and 50-51 under 35 U.S.C. 103(a) as being unpatentable over Volpe in view of Boyle and in further view of U.S. Publication No. 2005/0025315 ("Kreitzer") and [v] claims 14-18 under 35 U.S.C. 103(a) as being unpatentable over Volpe in view of Boyle and in further view of U.S. Patent No. 5,987,590 ("Wing").

VII. ARGUMENT

Below, the Appellant has provided arguments related with section headers in **bold**.

A. The 35 U.S.C. 112. 1st Paragraph Written Description Rejection of Claims 1, 12 and 14

Claims 1, 12 and 14 are rejected under 35 U.S.C. § 112, first paragraph, for allegedly failing to comply with the written description requirement.[1] Appellant respectfully traverses this rejection.

The Examiner indicated in the Advisory Action dated July 23, 2008 that the rejection of claims 1, 12 and 14 under 35 U.S.C. § 112, first paragraph will be withdrawn in view of Appellants remarks.[2] However, for completeness of the record Appellant will provide additional remarks below.

The Examiner alleges that the limitation "wherein the on-chip memory is selectably filled with data from an external memory **independent of cache accesses** of the cache memory" is not supported by the Specification as originally filed because the original Specification merely describes filling the on-chip memory with external data in advance of an eventual cache access.[3] Appellant respectfully disagrees with the Examiner's interpretation of this claim language.

Appellant directs the Appeals Board to Figure 3 of the Specification, which shows on-chip memory 350 connected to external main memory 360 via DME controller 352 and separately connected to cache memory 340 via DMA controller 344 and/or cache controller

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[1] See Pages 2-3 of the 5/2/2008 Final Office Action.
[2] See Continuation of 11 on the Continuation Sheet (PTO-303) of the 7/23/2008 Advisory Action.
[3] See Pages 2-3 of the 5/2/2008 Final Office Action., emphasis added.

342.[4] The connection between the on-chip memory 350 and the external main memory 360 is independent of the cache memory 340 in the sense that the cache memory 340 need not be involved in an interaction between the on-chip memory 350 and external main memory 360.[5]

As noted by the Examiner, one potential reason why a user would transfer data to the on-chip memory independent of a cache access "is that the user/programmer can arrange to have the instructions and data required by processor core 330 to be present in on-chip memory 350 well in advance of when they are actually needed by the processor core".[6] The Examiner's position appears to be that because data may be transferred to the on-chip memory in expectation of data, at some future point in time, being requested from the cache, the initial data transfer is dependent upon the later request.[7] Appellant respectfully disagrees.

Appellant submits that the actual user-controlled transfer of data to the on-chip memory 350 does not depend on an eventual cache access of the transferred data ever taking place. In other words, this transfer of data is not dependent on a cache-access. By contrast, if data were only loaded into the on-chip memory *in response* to a cache hit or miss, then the loading of the data would be dependent on the cache access. The fact that the transferred data may potentially aid a future scenario where a cache miss for the transferred data occurs does not make the earlier transfer of the data dependent on the cache access. This would be analagous to saying that packing clothes into luggage is dependent upon wearing the clothes at some later point in time, which is clearly not the case.

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[4] See Figure 3 of the Specification.
[5] E.g., see [0036] of the Specification.
[6] See [0037] of the Specification.
[7] See Pages 2-3 of the 5/2/2008 Final Office Action.

Further, the Examiner's reference to on-chip memory provided with data "in advance" of when it is needed is merely listed as an example of one advantage of an embodiment of the invention.[8] Nothing in the Specification says the eventual cache access *must* occur, or that the user will transfer the data only if it knows the eventual cache access will occur. For example, paragraph [0047] discusses how the on-chip memory 450 becomes the worst-case scenario for data retrieval, which means the on-chip memory 450 may be transferred data that is expected to be accessed, but is not actually accessed, unless the user transfers data with perfect foresight.[9]

In any case, Appellant submits that an earlier transfer of data to an on-chip memory is not dependent upon a processor looking for that data in a cache at some future point in time, and as such the claim language of "wherein the on-chip memory is selectably filled with data from an external memory independent of cache accesses of the cache memory" is supported by the Specification as originally filed.

Accordingly, in view of the foregoing, Appellant respectfully submits that the present application provides adequate written description of the claim limitation present in each of independent claims 1, 12 and 14, as acknowledged by the Examiner.[10] Appellant respectfully requests that the Appeals Board withdraw this rejection.

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[8] See [0037] of the Specification.
[9] See [0047] of the Specification.
[10] See Continuation of 11 on the Continuation Sheet (PTO-303) of the 7/23/2008 Advisory Action.

B. The 35 U.S.C. 103(a) Rejection of Claims 1-5, 7, 10-13, 35, 38-40, 43-46, 49 and 52-54 under 35 U.S.C. 103(a) based on Volpe in view of Boyle

The disputed claim language that is present within independent claim 1 and similarly in 12 is "wherein the on-chip memory is selectably filled with data from an external memory independent of cache accesses of the cache memory under user control".[11] As discussed in Appellants comments with respect to the 35 U.S.C. 112, 1st rejection provided above, this claim language means that data is transferred to the on-chip memory independent of, or not in response to, "cache accesses" of cache memory. As will be appreciated by one of ordinary skill in the art, a cache access may correspond to a cache hit or cache miss to the cache memory.

Volpe is directed to a prefetch buffer method and apparatus.[12] The Examiner reads the claimed "processor core" upon core processor 10 of Figure 1 of Volpe, the claimed "cache memory" upon L1 data memory of Figure 1 of Volpe, and the claimed "on-chip memory" upon prefetch buffer 260 of Figure 3 of Volpe.[13] Appellant agrees with the Examiner in that the prefetch buffer 260 fails to disclose "that the [prefetch buffer 260] is selectably filled with data from an external memory independent of cache access of cache memory under user control".[14] The Examiner alleges that Boyle discloses this particular deficiency of Volpe.[15]

As an initial matter, to avoid confusion, Appellant notes that the Patent No. listed for Boyle is incorrectly listed on page 3 of the 5/2/2008 final Office Action. Appellant's

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[11] See Page 2 of the 7/23/2008 Advisory Action.
[12] See Volpe, Abstract.
[13] See Pages 3-4 of the 5/2/2008 Final Office Action.
[14] See Page 4 of the 5/2/2008 Final Office Action.
[15] Id.

representative called Examiner Song on 6/11/2008, and Examiner Song indicated that the correct Patent No. for Boyle was 7,194,576.

The Examiner primarily cites to Figure 3 and steps 316-320 of Boyle as disclosing filling, with data, an on-chip memory independent of a cache access.[16] Appellant respectfully disagrees, and will now explain how Boyle's process of Figure 3 is entirely dependent upon a cache access.

Referring to Figure 3 of Boyle, in step 310, a cache controller 204 receives a request for either (i) an instruction code or (ii) non-instruction data.[17] Next, in step 312, the cache controller 204 checks a cache memory 207 to determine whether the requested data is already available.[18] If the data (i.e., either the instruction code or non-instruction data) is available, the data cache controller 204 simply loads and transfers the requested data from the cache memory 207 to the requesting entity.[19] If the requested data is not available in the cache, the cache controller 204 determines whether the data request is for non-instruction data.[20] If the data request is for non-instruction data, the cache controller 204 fetches the non-instruction data from a remote memory without actually updating the cache memory 207 to include the fetched data.[21] Thus, **in response to a cache miss**, Boyle teaches selectively updating the cache memory based on whether the requested data was an instruction code.

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[16] See Pages 4-5 of the 5/2/2008 Final Office Action.
[17] See Figure 3 and Column 3, lines 19-25 of Boyle.
[18] See Figure 3 and Column 3, lines 34-42 of Boyle.
[19] See Figure 3, step 312, and Column 3, lines 34-42 of Boyle.
[20] See Figure 3, step 314 of Boyle.
[21] See steps 316, 318 of Figure 3 of Boyle.

The reason for Boyle's cache-bypass at step 318 of Figure 3 is that instruction codes are more likely to repeat than non-instruction data.[22] Thus, it is better to reserve cache-space for instruction codes and only retrieve non-instruction data as needed because the data will be requested less frequently, and the size of the cache memory can thereby be reduced without significantly increasing cache miss latency.

Still, whether or not requested data is ever actually stored in the cache is largely irrelevant. In Boyle, the cache is accessed in steps 310/312 where the cache controller 204 determines whether the requested data is actually in the cache memory 207.[23] Clearly, this determination could not be made if the cache memory 207 were not accessed to determine a cache hit or miss. If there is a cache-hit, the data is simply provided from the cache.[24] If there is a cache miss, then instruction code is fetched and stored in the cache (implicit within Figure 3), whereas non-instruction data is simply fetched.[25] Each operation in Figure 3 is dependent upon first evaluating whether the requested data is actually in the cache, and this means the entire process of Figure 3 is dependent upon a cache access for the requested data. The mere fact that the cache is not necessarily accessed again at step 318 (although for instruction codes, it would be) does not negate the dependency of Figure 3 of Boyle upon the initial cache access, because steps 314-320 only occur if there is determined to be a cache miss.[26]

Because a cache miss clearly qualifies as a cache access, and the missing data is only fetched in response to the cache miss, Appellant respectfully submits that Volpe in view of Boyle cannot disclose or suggest "wherein the on-chip memory is selectably filled with data

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[22] See Column 3, line 58 to Column 4, line 11 of Boyle.
[23] See Column 3, lines 19-42, and Figure 3 of Boyle.
[24] See step 312 of Figure 3 of Boyle.
[25] See step 318 of Figure 3 of Boyle.
[26] See Figure 3 of Boyle and description thereof.

from an external memory independent of cache accesses of the cache memory under user control" as recited in independent claim 1 and similarly recited in independent claim 12.

As such, claims 2-5, 10-11, 13, 35, 38-40, 43-46, 49 and 52-54, dependent upon independent claims 1 and 12, respectively, are likewise allowable over Volpe in view of Boyle at least for the reasons given above with respect to independent claims 1 and 12.

Appellant respectfully requests that the Appeals Board withdraw this art grounds of rejection.**C. The 35 U.S.C. 103(a) Rejection of claim 8 based on Volpe, Boyle and Ramchandran.**

With respect to claim 8, which depends from independent claim 1, Ramchandran is directed to a cache for instruction set architecture using indexes to achieve compression.[27] A review of Ramchandran indicates that Ramchandran cannot cure the suggestion and disclosure deficiencies of Volpe in view of Boyle as discussed above with respect to independent claim 1.

As such, claim 8, dependent upon independent claim 1, is likewise allowable over Volpe in view of Boyle in further view of Ramchandran at least for the reasons given above with respect to independent claim 1.

D. The 35 U.S.C. 103(a) Rejection of claims 41-42 and 50-51 based on Volpe, Boyle and Kreitzer.

With respect to claims 41-42 and 50-51, which depend from independent claims 1 and 12, respectively, Kreitzer is directed to a method and apparatus for secure communications among portable communication devices.[28] A review of Kreitzer indicates that Kreitzer cannot

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[27] See Ramchandran, Abstract.
[28] See Kreitzer, Abstract.

cure the suggestion and disclosure deficiencies of Volpe in view of Boyle as discussed above with respect to independent claims 1 and 12.

As such, claims 41-42 and 50-51, dependent upon independent claims 1 and 12, respectively, are likewise allowable over Volpe in view of Boyle in further view of Kreitzer at least for the reasons given above with respect to independent claim 1. Appellant respectfully requests that the Appeals Board withdraw this art grounds of rejection.

E. The 35 U.S.C. 103(a) Rejection of claims 14-18 based on Volpe, Boyle and Wing

With respect to claims 14-18, Appellant respectfully submits that Volpe in view of Boyle cannot disclose or suggest "wherein the on-chip memory is selectably filled with data from an external memory ***independent of cache accesses of the cache memory*** under user control" as recited in independent claim 14, at least for the reasons set forth above with respect to independent claims 1 and 2. Further, Wing is directed to PC circuits, systems and methods.[29] A review of Wing indicates that Wing cannot cure the suggestion and disclosure deficiencies of Volpe in view of Boyle as discussed above with respect to independent claim 14.

As such, claims 15-18, dependent upon independent 14, are likewise allowable over Volpe in view of Boyle in further view of Wing at least for the reasons given above with respect to independent claim 14.

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[29] See Wing, Abstract.

Appellant respectfully requests that the Appeals Board withdraw this art grounds of rejection

For at least the reasons presented above, Appellant respectfully requests that the Board reverse the Examiner's rejections, and further requests issuance for the present application.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the Examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in Section II, above.

XI. CONCLUSION

The Appellant respectfully submits that claims 1-5, 7-8, 10-18 and 35-54 are patentable over the applied art and that all of the rejections and objections of record should be reversed.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 17-0026 for any additional fees required under 37 C.F.R. § 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

Dated: October 6, 2008 /Nicholas J, Pauley/

Nicholas J, Pauley
Reg. No. 44,999

QUALCOMM Incorporated
Attn: Patent Department
5775 Morehouse Drive
San Diego, California 92121
Telephone: (858) 845-4265
Facsimile: (858) 658-2502

APPENDIX A: CLAIMS

1. (Previously Presented) An integrated circuit (IC) comprising:

a processor core operable to perform data processing for the integrated circuit;

a cache memory operable to store data for the processor core; and

an on-chip memory operable to store data for the cache memory, wherein the cache memory is filled with data from the on-chip memory for cache misses, and wherein the on-chip memory is selectably filled with data from an external memory independent of cache accesses of the cache memory under user control.

2. (original) The integrated circuit of claim 1, further comprising:

a cache controller operable to handle memory transactions for the cache memory.

3. (original) The integrated circuit of claim 2, further comprising:

a direct memory exchange (DME) controller operable to handle data transfers between the on-chip memory and the external memory.

4. (original) The integrated circuit of claim 3, wherein the DME controller further operates with the cache controller to maintain data integrity for the cache memory.

5. (Previously Presented) The integrated circuit of claim 2, further comprising:

a direct memory access (DMA) controller operable to handle storage of DMA data received via at least one DMA channel to the cache memory or the on-chip memory, wherein the DMA controller further operates with the cache controller to maintain data integrity for the cache memory.

6. (cancelled)

7. (Previously Presented) The integrated circuit of claim 5, further comprising:

a direct memory exchange (DME) controller operable to handle data transfers between the on-chip memory and the external memory, wherein the DME controller couples to the DMA controller via at least one DMA channel.

8. (Previously Presented) The integrated circuit of claim 5, further comprising:

an internal memory bus coupling the on-chip memory, the cache controller, and the DMA controller, wherein the internal memory bus has a width that is equal to a line in the cache memory.

9. (cancelled)

10. (original) The integrated circuit of claim 1, wherein the cache memory and the on-chip memory are fabricated on same integrated circuit die.

11. (original) The integrated circuit of claim 1, wherein the cache memory and the on-chip memory are fabricated on different integrated circuit dies encapsulated within an IC package for the integrated circuit.

12. (Previously Presented) A wireless apparatus comprising:

an integrated circuit including

a processor core operable to perform data processing,

a cache memory operable to store data for the processor core, and

an on-chip memory operable to store data for the cache memory; and

an external memory operable to store data for the on-chip memory, wherein the cache memory is filled with data from the on-chip memory for cache misses, and wherein the on-chip memory is selectably filled with data from the external memory independent of cache accesses of the cache memory under user control.

13. (original) The integrated circuit of claim 12, further comprising:

a direct memory access (DMA) controller operable to handle storage of DMA data received via at least one DMA channel to the cache memory or the on-chip memory.

14. (Previously Presented) An integrated circuit comprising:

a first processor operable to perform general-purpose processing for the integrated circuit;

a second processor operable to perform data processing for the integrated circuit and including

a processor core operable to perform the data processing, and

a first cache memory operable to store data for the processor core;

an on-chip memory operable to store data for the first cache memory, wherein the first cache memory is filled with data from the on-chip memory for cache misses, and wherein the on-chip memory is selectably filled with data from an external memory independent of cache accesses of the first cache memory under user control; and

a first memory bus coupling the first and second processors to the external memory.

15. (Previously Presented) The integrated circuit of claim 14, wherein the second processor further includes a second cache memory operable to store instructions for the processor core, and wherein the second cache memory is automatically filled with instructions from the on-chip memory for cache misses.

16. (original) The integrated circuit of claim 15, wherein the second processor further includes

a first cache controller operable to handle memory transactions for the first cache memory,

a second cache controller operable to handle memory transactions for the second cache memory,

a direct memory access (DMA) controller operable to handle storage of DMA data received via at least one DMA channel to the first cache memory, the second cache memory, or the on-chip memory, and

a direct memory exchange (DME) controller operable to handle data transfers between the on-chip memory and the external memory.

17. (original) The integrated circuit of claim 16, wherein the DMA controller and the DME controller further operate with the first and second cache controllers to maintain data integrity for the first and second cache memories.

18. (Previously Presented) The integrated circuit of claim 16, wherein the second processor further includes a second memory bus coupling the on-chip memory, the first and second cache controllers, and the DMA controller, and wherein the DME controller couples to the DMA controller via at least one DMA channel.

19 - 34. (cancelled).

35. (Previously Presented) The integrated circuit of claim 3, wherein the DME controller is selectably programmable by the user to fill the on-chip memory with data from the external memory independent of the cache misses, to thereby provide the user control.

36. (Previously Presented) The integrated circuit of claim 35, further comprising:

a shared memory bus connected to the DME controller and the external memory; and

a direct memory access (DMA) controller coupled to the cache controller, an internal memory bus, and said shared memory bus, wherein said DMA controller has a plurality of DMA channels that can receive high-rate DMA data by way of the shared memory bus or the internal memory bus.

37. (Previously Presented) The integrated circuit of claim 36, wherein the DME controller couples to at least one of the plurality of DMA channels, and said DME controller is selectably programmable to fill the on-chip memory with data from the external memory by paging blocks of instructions or data.

38. (Previously Presented) The integrated circuit of claim 3, wherein the DME controller is selectably programmable by a user to schedule the filling of on-chip memory with data from the external memory.

39. (Previously Presented) The integrated circuit of claim 3, wherein the DME controller is selectably programmable by the user to control the filling of the on-chip memory with data blocks from the external memory such that the user functions as an anticipatory cache controller.

40. (Previously Presented) The integrated circuit of claim 3, wherein the DME controller is selectably programmable by the user to fill the on-chip memory with data from the external memory well in advance of need by the processor core and without paging-on-demand.

41. (Previously Presented) The integrated circuit of claim 1, wherein said integrated circuit is operable in a wireless device, said wireless device comprising:

an antenna to wirelessly communicate signals with a remote base station;

a receiver unit operably connected to said antenna and said integrated circuit to communicate a received signal from said antenna to said integrated circuit; and

a transmitter unit operably connected to said antenna and said integrated circuit to communicate data from said integrated circuit to said antenna as a transmission signal.

42. (Previously Presented) The integrated circuit of claim 1, wherein said integrated circuit is operable in a wireless device, said wireless device comprising:

means for communicating data between said integrated circuit and a remote base station.

43. (Previously Presented) The integrated circuit of claim 1, further comprising:

means for handling data transfers between the on-chip memory and the external memory, said means being selectably programmable by a user to fill the on-chip memory with data from the external memory independent of the cache misses.

44. (Previously Presented) The integrated circuit of claim 43, wherein said means is programmable to page blocks of instructions and/or data between the on-chip memory and the external memory.

45. (Previously Presented) The integrated circuit of claim 43, wherein said means is programmable to schedule the filling of the on-chip memory with data from the external memory.

46. (Previously Presented) The wireless apparatus of claim 12, further comprising:

a direct memory exchange (DME) controller operable to handle data transfers between the on-chip memory and the external memory.

47. (Previously Presented) The wireless apparatus of claim 12, further comprising:

a shared memory bus connected to the DME controller and the external memory; and

a direct memory access (DMA) controller coupled to a cache controller, an internal memory bus, and said shared memory bus, wherein said DMA controller has a plurality of DMA channels that can receive high-rate DMA data by way of the shared memory bus or the internal memory bus.

48. (Previously Presented) The wireless apparatus of claim 46, wherein said DME controller couples to at least one of a plurality of DMA channels, and said DME controller is selectably programmable to fill the on-chip memory with data from the external memory by paging blocks of instructions or data.

49. (Previously Presented) The wireless apparatus of claim 12, wherein the DME controller is selectably programmable by a user to schedule the filling of on-chip memory with data from the external memory.

50. (Previously Presented) The wireless apparatus of claim 12, further comprising:

an antenna to wirelessly communicate signals with a remote base station;

a receiver unit operably connected to said antenna and said integrated circuit to communicate a received signal from said antenna to said integrated circuit; and

a transmitter unit operably connected to said antenna and said integrated circuit to communicate data from said integrated circuit to said antenna as a transmission signal.

51. (Previously Presented) The wireless apparatus of claim 12, further comprising:

means for communicating data between said integrated circuit and a remote base station.

52. (Previously Presented) The wireless apparatus of claim 12, further comprising:

means for handling data transfers between the on-chip memory and the external memory, said means being selectably programmable by a user to fill the on-chip memory with data from the external memory independent of the cache misses.

53. (Previously Presented) The wireless apparatus of claim 52, wherein said means is programmable to page blocks of instructions and/or data between the on-chip memory and the external memory.

54. (Previously Presented) The wireless apparatus of claim 52, wherein said means is programmable to schedule the filling of the on-chip memory with data from the external memory.

APPENDIX B: EVIDENCE

(None)

APPENDIX C: RELATED PROCEEDINGS

(None)